CLAIM AMENDMENTS

Please cancel claims 3-4 without prejudice or disclaimer.

Please amend claims 1-2 and 5-14 as follows.

1. (Currently Amended) A memory cell comprising:

a first inverter comprising a first pull-up transistor, the first pull-up transistor comprising a first body terminal;

a second inverter cross-coupled to the first inverter and comprising a second pull-up transistor comprising a second body terminal; and

a switch connected to the first and second body ~~bodies~~ terminals, the switch to couple the first and the second body terminals to a forward body bias voltage.

2. (Currently Amended) The memory cell as set forth in claim 1, the memory cell further comprising a power rail and a ground rail, wherein

the first pull-up transistor of the first inverter is a first pFET, further comprising a first source terminal connected to the power rail, a first gate terminal, and a first drain terminal;

the first inverter further comprises a first pull-down nFET comprising a second drain terminal connected to the first drain terminal of the first pFET of the first inverter, comprising a second gate terminal, and comprising a second source terminal connected to the ground rail;

the second pull-up transistor of the second inverter is a second pFET, further comprising a third source terminal connected to the power rail, a third gate terminal, and a third drain terminal;

the second inverter further comprises a second pull-down nFET comprising a fourth drain terminal connected to the third drain terminal of the second pFET of the second inverter, comprising a fourth gate terminal, and comprising a fourth source terminal connected to the ground rail; and

wherein the first and second gates of the first pFET and the first nFET, respectively, of the first inverter are connected to the third drain of the second pFET of the second inverter, and the third and fourth gates of the second pFET and the second nFET,

respectively, of the second inverter are connected to the first drain of the first pFET of the first inverter.

3. (Canceled).

4. (Canceled).

5. (Currently Amended) A memory cell comprising:

a first inverter comprising a first pull-up transistor, the first pull-up transistor comprising a first body; and

a second inverter cross-coupled to the first inverter and comprising a second pull-up transistor comprising a second body;

wherein the first and second bodies are forward biased.

6. (Currently Amended) The memory cell as set forth in claim 5, the memory cell further comprising a power rail and a ground rail, wherein

the first pull-up transistor of the first inverter is a first pFET, further comprising a first source terminal connected to the power rail, a first gate terminal, and a first drain terminal;

the first inverter further comprises a first pull-down nFET comprising a second drain terminal connected to the first drain terminal of the first pFET of the first inverter, comprising a second gate terminal, and comprising a second source terminal connected to the ground rail;

the second pull-up transistor of the second inverter is a second pFET, further comprising a third source terminal connected to the power rail, a third gate terminal, and a third drain terminal;

the second inverter further comprises a second pull-down nFET comprising a fourth drain terminal connected to the third drain terminal of the second pFET of the second inverter, comprising a fourth gate terminal, and comprising a fourth source terminal connected to the ground rail; and

wherein the first and second gates of the first pFET and the first nFET, respectively, of the first inverter are connected to the third drain of the pFET of the second

inverter, and the third and fourth gates of the second pFET and the second nFET, respectively, of the second inverter are connected to the first drain of the first pFET of the first inverter.

7. (Currently Amended) A memory comprising:

a cell comprising:

a first inverter comprising a first pull-up transistor comprising a first body terminal and a first source terminal; and

a second inverter comprising a second pull-up transistor comprising a second body terminal and a second source terminal, wherein the first and second inverters are cross-coupled to each other;

wherein the first and second source terminal are coupled to a power rail, the power rail having ~~to provide~~ a voltage Vcc ~~to the source terminals~~; and

wherein the first and second body terminals are coupled to a bias voltage generator, the bias voltage generator having ~~to provide~~ a voltage Vb ~~to the body terminals~~, wherein Vb < Vcc.

8. (Currently Amended) The memory as set forth in claim 7, further comprising:

a switch ~~coupled~~ to couple the voltage Vb of the bias voltage generator **[[**and**]]** to the first and second body terminals ~~so that the bias voltage generator provides the voltage Vb to the body terminals~~ during a read operation on the memory cell.

9. (Currently Amended) The memory as set forth in claim 8, the memory comprising a ground rail, the ground rail having ~~to provide~~ a voltage Vss, where Vss < Vb, wherein

the first pull-up transistor of the first inverter is a first pFET, further comprising a first gate terminal and a first drain terminal;

the first inverter further comprises a first pull-down nFET comprising a second drain terminal connected to the first drain terminal of the first pFET of the first inverter, the first pull-down nFET comprising a second gate terminal, and comprising a second source terminal connected to the ground rail;

the second pull-up transistor of the second inverter is a second pFET, further comprising a third gate terminal and a third drain terminal;

the second inverter further comprises a second pull-down nFET comprising a fourth drain terminal connected to the third drain terminal of the second pFET of the second inverter, comprising a fourth gate terminal, and comprising a fourth source terminal connected to the ground rail; and

wherein the first and second gates of the first pFET and the first nFET, respectively, of the first inverter are connected to the third drain of the pFET of the second inverter, and the third and fourth gates of the second pFET and the second nFET, respectively, of the second inverter are connected to the first drain of the first pFET of the first inverter.

10. (Currently Amended) The memory as set forth in claim 7, the memory comprising a ground rail, the ground rail having ~~to provide~~ a voltage Vss, where Vss < Vb, wherein

the first pull-up transistor of the first inverter is a first pFET, further comprising a first gate terminal and a first drain terminal;

the first inverter further comprises a first pull-down nFET comprising a second drain terminal connected to the first drain terminal of the first pFET of the first inverter, the first pull-down nFET comprising a second gate terminal, and comprising a second source terminal connected to the ground rail;

the second pull-up transistor of the second inverter is a second pFET, further comprising a third gate terminal and a third drain terminal;

the second inverter further comprises a second pull-down nFET comprising a fourth drain terminal connected to the third drain terminal of the second pFET of the second inverter, comprising a fourth gate terminal, and comprising a fourth source terminal connected to the ground rail; and

wherein the first and second gates of the first pFET and the first nFET, respectively, of the first inverter are connected to the third drain of the second pFET of the second inverter, and the third and fourth gates of the second pFET and the second nFET, respectively, of the second inverter are connected to the first drain of the first pFET of the first inverter.

11. (Currently Amended) A system comprising:

a first die comprising a functional unit;

a second die comprising a processor, the second die distinct from the first die, the second die comprising:

a memory cell, the cell comprising:

a first inverter comprising a first pull-up transistor comprising a first body terminal and a first source terminal; and

a second inverter comprising a second pull-up transistor comprising a second body terminal and a second source terminal, wherein the first and second inverters are cross-coupled to each other;

a power rail coupled to the first and second source terminals, power rail having ~~to provide~~ a voltage Vcc ~~to the source terminals~~; and

a bias voltage generator coupled to the first and second body terminals, the bias voltage generator having ~~to provide~~ a voltage Vb ~~to the body terminals~~, wherein Vb < Vcc.

12. (Currently Amended) The system as set forth in claim 11, the second die further comprising:

a switch ~~coupled~~ to couple the voltage Vb of the bias voltage generator **[[**and**]]** to the first and second body terminals ~~so that the bias voltage generator provides the voltage Vb to the body terminals~~ during a read operation on the memory cell.

13. (Currently Amended) The system as set forth in claim 12, the second die further comprising a ground rail having ~~to provide~~ a voltage Vss, where Vss < Vb, wherein

the first pull-up transistor of the first inverter is a first pFET, further comprising a first gate terminal and a first drain terminal;

the first inverter further comprises a first pull-down nFET comprising a second drain terminal connected to the first drain terminal of the first pFET of the first inverter, comprising a second gate terminal, and comprising a second source terminal connected to the ground rail;

the second pull-up transistor of the second inverter is a second pFET, further comprising a third gate terminal and a third drain terminal;

the second inverter further comprises a second pull-down nFET comprising a fourth drain terminal connected to the third drain terminal of the second pFET of the second

inverter, the second pull-down nFET comprising a fourth gate terminal, and comprising a fourth source terminal connected to the ground rail; and

wherein the first and second gates of the first pFET and the first nFET, respectively, of the first inverter are connected to the third drain of the second pFET of the second inverter, and the third and fourth gates of the second pFET and the second nFET, respectively, of the second inverter are connected to the first drain of the first pFET of the first inverter.

14. (Currently Amended) The system as set forth in claim 11, the second die further comprising a ground rail to provide a voltage Vss, where Vss < Vb, wherein

the first pull-up transistor of the first inverter is a first pFET, further comprising a first gate terminal and a first drain terminal;

the first inverter further comprises a first pull-down nFET comprising a second drain terminal connected to the first drain terminal of the first pFET of the first inverter, the first pull-down nFET comprising a second gate terminal, and comprising a second source terminal connected to the ground rail;

the second pull-up transistor of the second inverter is a second pFET, further comprising a third gate terminal and a third drain terminal;

the second inverter further comprises a second pull-down nFET comprising a fourth drain terminal connected to the third drain terminal of the second pFET of the second inverter, comprising a fourth gate terminal, and comprising a fourth source terminal connected to the ground rail; and

wherein the first and second gates of the first pFET and the first nFET, respectively, of the first inverter are connected to the third drain of the second pFET of the second inverter, and the third and fourth gates of the second pFET and the second nFET, respectively, of the second inverter are connected to the first drain of the first pFET of the first inverter.